

Bottom-Gate Approach for All Basic Logic Gates Implementation by a Single-Type IGZO-Based MOS Transistor with Reduced Footprint

Shaocheng Qi, Joao Cunha, Tian-Long Guo, Peiqin Chen, Remo Proietti Zaccaria,* and Mingzhi Dai*

Logic functions are the key backbone in electronic circuits for computing applications. Complementary metal-oxide-semiconductor (CMOS) logic gates, with both n-type and p-type channel transistors, have been to date the dominant building blocks of logic circuitry as they carry obvious advantages over other technologies. Important physical limits are however starting to arise, as the transistor-processing technology has begun to meet scaling-down difficulties. To address this issue, there is the crucial need for a next-generation electronics era based on new concepts and designs. In this respect, a single-type channel multigate MOS transistor (SMG-MOS) is introduced holding the two important aspects of processing adaptability and low static dissipation of CMOS. Furthermore, the SMG-MOS approach strongly reduces the footprint down to 40% or even less area needed for current CMOS logic function in the same processing technology node. Logic NAND, NOT, AND, NOR, and OR gates, which typically require a large number of CMOS transistors, can be realized by a single SMG-MOS transistor. Two functional examples of SMG-MOS are reported here with their analysis based both on simulations and experiments. The results strongly suggest that SMG-MOS can represent a facile approach to scale down complex integrated circuits, enabling design flexibility and production rates ramp-up.

Complementary metal-oxide-semiconductor (CMOS) transistors are one of the dominating components in the modern logic gate family as they are characterized by a remarkable adaptability to modern foundry lines and low leakage current, which ensure high fabrication reliability/repeatability and low power dissipation, respectively.^[4,5]

For CMOS logic gates, a minimum number of two metal-oxide-semiconductor (MOS) field-effect transistors (FETs) are required to achieve the simplest Boolean logic gate, the logic NOT (Figure 1). Specifically, an n-type channel MOS (NMOS) field-effect transistor (FET) and a p-type channel MOS (PMOS) FET are used. CMOS logic gates are built by employing two different semiconductor materials, resulting in material and processing complexity. Furthermore, to accomplish two-input Boolean logic gates with CMOS requires more than two transistors. According to the well-known Moore's law, the number of transistors per square inch on an IC should be dou-

bled every two years, which is equivalent to scaling down the dimension of each transistor by half. Until recent years, this steady technological advancement allowed for an equally steady improvement of computers performance, especially in terms of

1. Introduction

Logic function gates are the basic and fundamental elements enabling data processing in electronic integrated circuits (IC).^[1–6]

S. Qi
School of Materials Science and Engineering
Shanghai University
Shanghai 200444, China

S. Qi, P. Chen, Prof. M. Dai
Ningbo Institute of Materials Technology and Engineering
Chinese Academy of Sciences
Ningbo 315201, P. R. China
E-mail: daimz@nimte.ac.cn

 The ORCID identification number(s) for the author(s) of this article can be found under <https://doi.org/10.1002/advs.201901224>.

© 2020 The Authors. Published by WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim. This is an open access article under the terms of the Creative Commons Attribution License, which permits use, distribution and reproduction in any medium, provided the original work is properly cited.

DOI: 10.1002/advs.201901224

J. Cunha, Dr. T.-L. Guo, Prof. R. Proietti Zaccaria
Cixi Institute of Biomedical Engineering
Ningbo Institute of Materials Technology and Engineering
Chinese Academy of Sciences
Ningbo 315201, China
E-mail: remo.proietti@nimte.ac.cn

J. Cunha
University of Chinese Academy of Sciences
Beijing 100049, China

Prof. R. Proietti Zaccaria
Istituto Italiano di Tecnologia
via Morego 30, 16163 Genoa, Italy

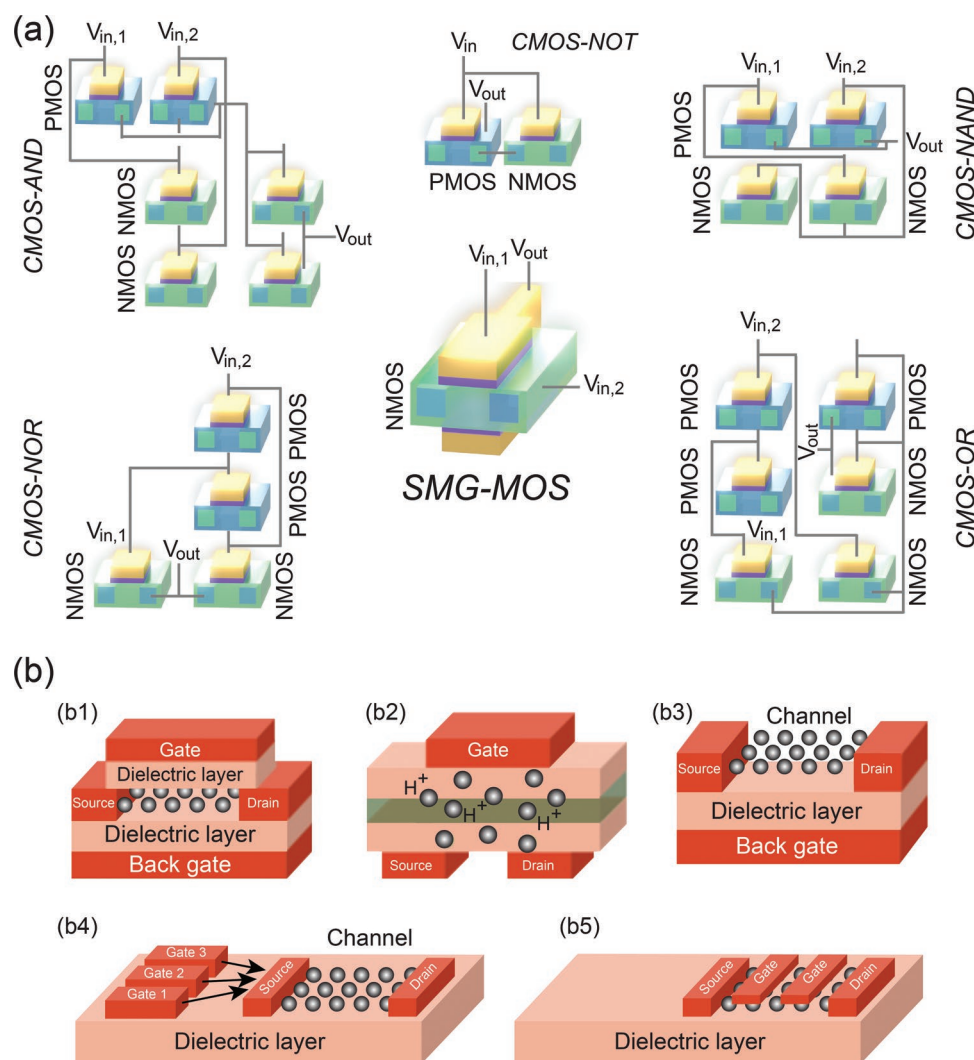


Figure 1. Comparison of CMOS logic circuits and SMG-MOS circuit. a) The SMG-MOS circuit shows a footprint about 40% of a CMOS circuit performing the same logic function. These schematics follow the foundry line (top gate approach). b) Schematic comparison of bottom gate-like solutions employing external-channel (i.e., not directly connected to the channel) gates (b1–b4) with our internal-channel (i.e., directly connected to the channel) gate approach (b5). In particular, (b1) is a representation of the device concept from ref. [36], (b2) from refs. [37–39], (b3) from refs. [40,41], and (b4) from refs. [42–45]. Finally, (b5) shows the configuration proposed in the present work. Importantly, this configuration employs a reduced number of material layers than (b1–b3) and a lower surface coverage than (b4).

computational speed. A scaled down circuit can indeed enable a faster logic data transporting and processing. However, lithographic techniques constraining quantum effects and limited dopant placement capabilities have currently begun to interfere with Moore's law.

To extend the benefits of the Moore's law, highly complex and expensive innovative fabrication processes as well as new logical schemes are required.^[1–8] In this regard, several different alternative logic gates have been investigated,^[9–33] such as nanotube gates,^[9–13] 2D materials logic gates,^[15–18] quantum logic gates,^[19–23] and biocircuits.^[26–28] For instance, quantum logic gates are scalable using existing silicon technologies, but they demand very low working temperatures.^[22–25] Biocircuits employ biological elements, which are difficult to control and are highly sensitive to working conditions including temperature, with the drawback of not being suitable for nowadays

foundry processing lines since they require very different fabrication equipment facilities very different from the existing semiconductor foundry product lines.^[26,27] Several of these alternatives share this drawback failing the important requirement of relying on the present processing schemes as many of the proposed designs are undeveloped trials which are not immediately implementable.^[34,35] Rather than updating the processing, materials and working environments, the manipulations of the transistor design provides an easier and cheaper approach as it can be implemented via an easy and simple modification of existing manufacturing tools and recipes.

Here, we design, fabricate, characterize, and simulate a single-type channel multigate MOS transistor (SMG-MOS) meeting the requirements of scaling down capability, low static power dissipation, and compatibility with nowadays foundry lines, where no extra instruments and processing are required.

A single SMG-MOS transistor can work as different basic Boolean logic gates, such as NAND, NOT, AND, NOR, and OR, which otherwise would require a large number of CMOS transistors (Figure 1). The different logic functions are obtained by producing different electric field profiles along the channel, which can be controlled by adjusting both the positioning of the transistor electrodes contacts along the channel and the applied voltages. Indeed, the SMG-MOS design utilizes a single-type channel structure with an output electrode added directly inside the channel, fabricated through a single-type channel transistor processing. The simplicity and functionality of the present SMG-MOS design results in a facile approach for scaling down integrated circuits. Indeed, it significantly decreases the number of transistors typically required for a logic circuit hence reducing the 2D footprint, power consumption, and cost while increasing processing speed and ensuring mass production capability. Importantly, the proposed architecture is profoundly different from standard double/multigate solutions both in terms of geometrical design and working principle. Specifically, in terms of geometrical design, in our proposed architecture a gate is added inside the channel (i.e., directly connected to it) whereas in standard double- or multigate structures a gate is added outside the channel (i.e., there is no direct connection to the channel). Furthermore, in terms of working mechanism, while standard double/multi-gate solutions are based on a not-localized electric field generation in the overall channel, where the side gates are used to control the channel, in our proposed design we use only specific portions of the channel to operate the output (i.e., the portion of the channel at the drain side is used to assign status 1 to the output, and the portion of the channel at the source side to assign status 0 to the output). These are fundamental differences leading to an important footprint reduction for our SMG-MOS design. For clarity, a visual representation of the illustrated concept is shown in Figure 1b.

2. Results and Discussion

2.1. SMG-MOS Fabrication and Logical Description

In this study, we implement a research lab line approach to realize the SMG-MOS concept, with the employment of a bottom gate as shown in Figure 2 in order to simplify the fabrication conditions. This approach is slightly different from the SMG-MOS shown in Figure 1 that instead depicts a foundry line approach. As shown in Figure 2a, the transistor is formed by drain (D), source (S), and output (O) electrodes with the semiconductor channel highlighted in blue and red colors. These elements are located on the top of a 100 nm thick SiO₂ layer. The layer electrically insulates the elements and an n-type silicon bottom gate (sheet resistance $\ll 0.005 \Omega \text{ cm}^2$). The semiconductor channel, with a thickness between 20 and 50 nm, is an n-type In-Ga-Zn-O (IGZO). IGZO is an amorphous oxide semiconductor (AOS) composite widely investigated and utilized in the thin film transistors (TFTs) field especially for displays and sensors.^[46–48,51,53] The electrodes are composed of a 60 nm thick Ni/Au alloy. The overall structure was fabricated following standard top-down fabrication

techniques. The details of the fabrication process can be found in the Experimental Section as well as in previous publications.^[46–53] Figure 2b,e shows the SEM images of the fabricated SMG-MOS devices, where the former highlights the smallest semiconductor channel with 200 nm width we could fabricate, and the latter represents the typical structure employed in our characterization.

We defined V_{GS} as the gate-to-source voltage, V_{out} as the output voltage, V_{DS} as the drain-to-source voltage and I_{DS} as the channel current measured from the drain terminal. Here, V_{GS} can be further specified as bottom gate voltage V_{BG} or side gate voltage V_{SG} . The threshold voltage of V_{BG} is defined as V_{Th} . A simplified nomenclature associates V_{in} to V_{GS} . If two inputs are required (depending on the considered logic gate), $V_{in,1}$ and $V_{in,2}$ will be considered corresponding to V_{BG} and V_{SG} , respectively, as also revealed in Figure 1. Regarding operation conditions, for both V_{in} and V_{out} , we define the logic condition 1 with a voltage value no less than 0.7 V.^[14] In turn, a voltage value lower than 0.7 V corresponds to logic 0.

Bearing this in mind, when a standard CMOS logic NOT circuit is considered (Figure 1), if V_{in} corresponding to logic 0 is applied, V_{out} is “pulled up” to logic 1 by the PMOS transistor. On the other hand, if V_{in} of logic 1 is applied, V_{out} is “pulled down” to logic 0 by the NMOS transistor.^[4] Differently from the CMOS logic design, the SMG-MOS assigns the output close to the drain, to “pull up” the output by the drain and “pull down” the output by the source (Figure 2b). By doing so, the output-to-drain part of the channel, named L_{OD} , could be turned on before the entire channel. Hence, different output values and thus logic gate functions could be implemented with careful positioning of the output. In the SMG-MOS logic NOT (Figure 2a), when V_{in} is a logic 0, the L_{OD} is turned on. This will enable V_{out} to be pulled up by V_{DS} to a voltage value more than 0.7 V, meaning V_{out} logic 1.^[21] On the contrary, when V_{in} is a logic 1, the output-to-source section L_{OS} is turned on, which connects V_{out} to the grounded source and shifts output to logic 0. Figure 2c shows the dependence of V_{out} and the channel current I_{DS} on V_{in} producing the function of a logic NOT (inverter). A detailed description of the overall mechanism is provided by Figure S1 (Supporting Information) and related text. Based on the same working principle, the SMG-MOS logic NOT was also capable of driving the second stage in a two-stage NOTs, producing similar results to CMOS NOT stages (Figure S2, Supporting Information).

For the remaining Boolean logic gates (Figure 1a), two inputs are required ($V_{in,1}$ and $V_{in,2}$). In order to fulfill this requirement, we add a side gate (SG) to the SMG-MOS NOT component shown in Figure 2d. A representative top-view SEM image is presented in Figure 2e. All basic Boolean logic gates can be implemented. In this respect, the SMG-MOS V_{out} as a function of the two inputs $V_{in,1}$ and $V_{in,2}$ for the four basic logic gates is shown in Figure 2f (NOR), Figure 2g (NAND), Figure 2h (OR), and Figure 2i (AND). Furthermore, V_{SG} is shown to enable the control of V_{Th} , which defines the “activate” condition of the channel (Figure S3, Supporting Information). In Figure 2a, number of different voltage conditions are shown, each of them associated with a specific logic gate. Generally speaking, for a relatively small drain and gate voltages, the AND logic gate can be implemented, whereas for a relatively high drain and gate voltages, the OR logic gate can be implemented.

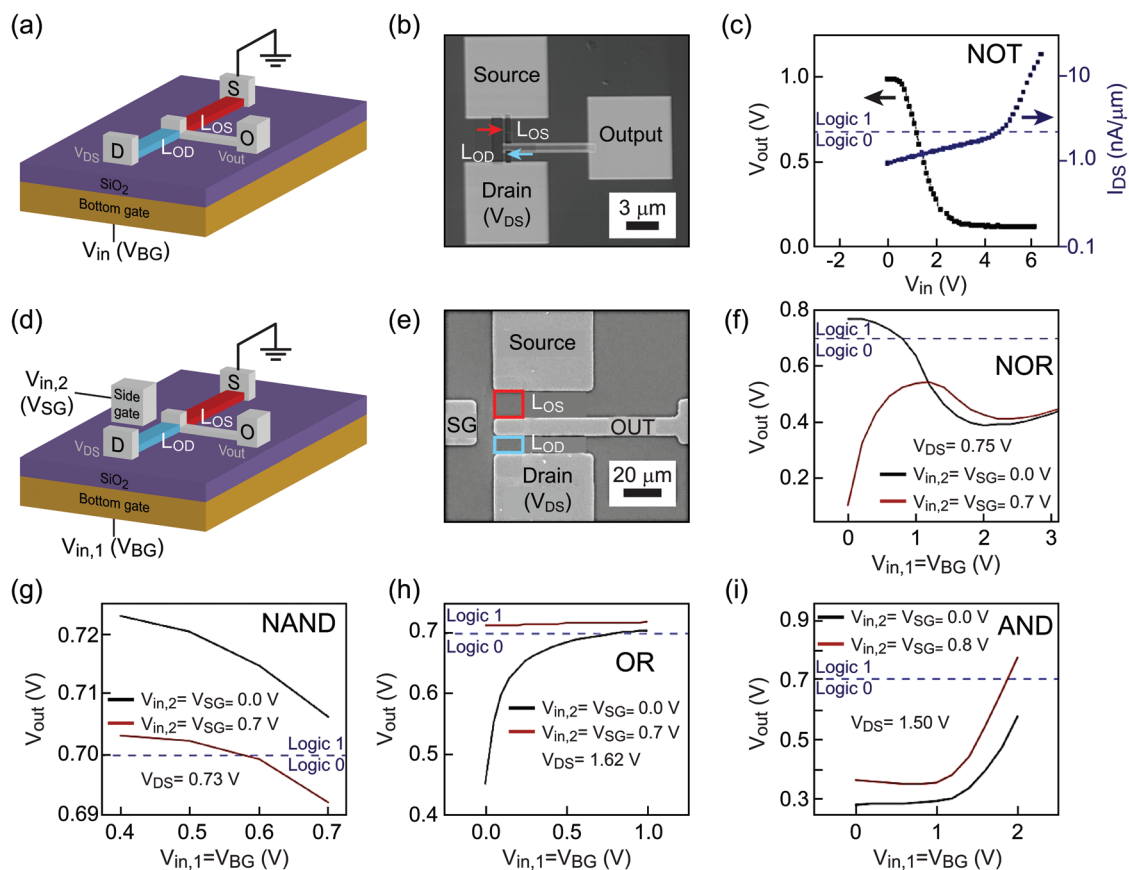


Figure 2. SMG-MOS transistor configuration. a) 3D illustration of a SMG-MOS logic NOT, with the bottom gate voltage V_{BG} (V_{in}), the source (S), the drain (D), the semiconductor channel (light blue and red color) and the output (O). The figure highlights the different length between L_{OS} and L_{OD} . b) SEM image of a SMG-MOS logic NOT (channel width = 200 nm, channel thickness = 10 nm). L_{OS} is the channel section comprised between the output and the source, and L_{OD} is the channel section comprised between the output and the drain. c) Plots of the output voltage (V_{out}) and channel current (I_{DS}) as a function of V_{in} . d) 3D illustration of a two-input SMG-MOS logic gate capable of addressing any other Boolean gates besides NOT. SG denotes a side gate providing the side gate voltage (V_{SG}), i.e., the second input $V_{in,2}$. e) SEM top-view of the two-input logic gate (channel thickness = 30 nm). f–i) Plots of V_{out} as a function of $V_{in,1}$ with $V_{in,2}$ taken as parameter for the logic gates NOR (f), NAND (g), OR (h), and AND (i).

Finally and for comparison purposes, the representative standard Boolean NMOS logic gates are shown schematically in Figure S4a (Supporting Information) while the corresponding SMG-MOS design is illustrated in Figure S4b (Supporting Information) with the associated truth tables in Figure S4c (Supporting Information). These results suggest that a single SMG-MOS can implement all basic Boolean operations, while performance improvement can be achieved by advanced lithography and proper material selection.

2.2. Mechanism Investigation

The mechanism underneath our design is revealed in a quantitative way through the electrical measurements shown in Figure 3.^[42] In SMG-MOS logic NOT, a reference voltage V_{ref} was applied to either the source or drain while V_{out} was measured to confirm the proper connection among the electrodes (Figure 3a). The increase of V_{out} (blue line) with V_{ref} applied to the drain confirms there is an electrical connection between the drain, implying L_{OD} is turned on. On the other hand, when V_{ref} is applied to the source, V_{out} (black line) remains constant,

confirming there is no connection between the source and output electrodes and demonstrating L_{OS} is turned off. The presence/absence of an electrical connection describes a logic NOT gate function. In this regard, TCAD simulations have been performed to determine the contribution to the V_{out} values coming from L_{OD} and L_{OS} .^[52,53] Simulation results (simulation parameters in Figure S5, Supporting Information) are found to fit well the experimental results in Figure 3b. A schematic illustration with the electric potential distribution along the channel as obtained from TCAD simulations is shown in Figure 3c,d. In particular, the contour plot in Figure 3c shows high electrical potential exclusively concentrated on the drain side when V_{in} = logic 0 ($V_{in} < V_{TH}$), which confirms previous discussion. As seen in Figure 3c, when the transistor is turned off then almost the entire channel is without carriers or associated appreciable electric field. In fact, only the electric field at the drain side, due to the high drain voltage stress, is strong enough to turn on that specific portion of the channel (drain side). In particular, if the output electrode is close enough to the drain, then only L_{OD} is turned on meaning a high localized electric field in the channel at the drain side. On the other hand, the remaining portion of the transistor channel remains in off condition, meaning a

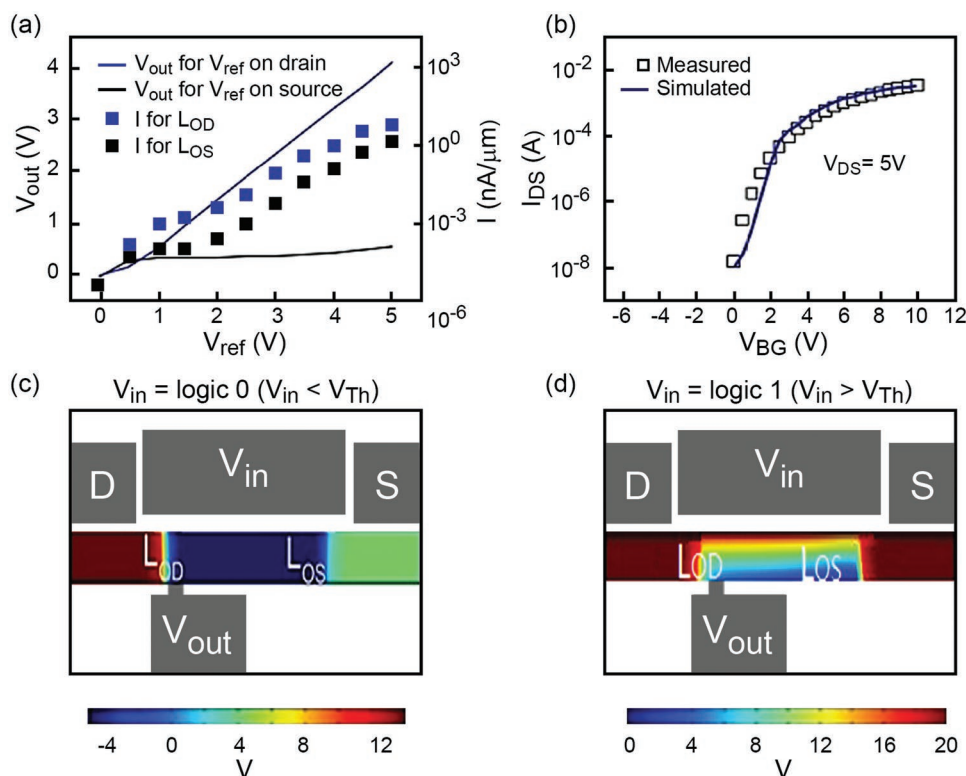


Figure 3. Mechanism of SMG-MOS logic NOT gate function. a) V_{out} versus reference voltage V_{ref} applied either on the drain (blue line) or source (black line). V_{out} is lower than V_{ref} when V_{ref} is applied to the source, which confirms the isolation between the output and the source when the input $V_{in} = \text{logic 0}$ ($V_{in} < V_{Th}$). The dotted data show that the channel current is lower than the leakage current of $100 \text{ nA } \mu\text{m}^{-1}$. b) Comparison between simulated (line) and experimental (scatter points) of I_{DS} vs V_{BG} . c) Schematic representation of simulated electric potential along the channel at $V_{in} = \text{logic 0}$, with only L_{OD} being activated. d) Schematic diagram of simulated potential at $V_{in} = \text{logic 1}$, with the activation of the entire channel.

low electric field in the rest of the channel and hence low current. The overall situation results in the channel undergoing on/off states for L_{OD} and L_{OS} , respectively. Additionally, the electric potential extends along the whole channel when $V_{in} = \text{logic 1}$ ($V_{in} > V_{Th}$) which suggests that the electrical connection between the output and the source induces $V_{out} = \text{logic 0}$ (Figure 3d). This localized distribution of potential confirms the working mechanism of SMG-MOS logic NOT.

In general, SMG-MOS logic operations can be explained using the band diagram formulation.^[4] In equilibrium conditions, there is no current flow along the channel given the existence of an energy barrier between the Fermi level E_F and the conduction band E_c . However, when E_c is pulled down below E_F due to an applied voltage bias, the conduction band carriers turn into mobile channel carriers.^[4] In this respect, either V_{GS} (side gate or bottom gate voltage) or V_{DS} can bend E_c and thus adjust V_{out} through the modification of the channel conductivity. **Figure 4a** shows E_c along the whole channel and how it is bent in a uniform way by applying a V_{GS} bias. The resulting channel current I_{DS} is depicted in **Figure 4b**. Different from V_{GS} , the quantity V_{DS} can control E_c only on the drain edge, as shown schematically in **Figure 4c**. Therefore, for high values of V_{DS} , only L_{OD} is turned on,^[54] leading to a short circuit between the output and drain and pulling up V_{out} to logic 1 with $V_{in} = \text{logic 0}$. This situation is suitable for the implementations of logic NOT, logic NAND, or logic NOR, which require V_{out} to be logic 1 when $V_{in} = \text{logic 0}$.

From **Figure 4d**, a typical output curve of an n-type transistor is shown. Two distinct behaviors can be retrieved when the channel is on: a linear behavior (zone I) followed by a flat behavior (zone II). The zone I corresponds to the electric field distributed along the channel in an average way so that the entire channel behaves like a resistor. In this case, the channel resistance and thus V_{DS} is linearly dependent on the channel length. The zone II, on the other hand, describes a situation where the channel at the drain edge is in saturation condition. The L_{OD} connection leads to $V_{out} = \text{logic 1}$ whereas the remaining part of the channel L_{OS} , not being in saturation condition, leads to $V_{out} = \text{logic 0}$.^[4] Therefore, $V_{out} = \text{logic 1}$ generally could occur in three cases: i) when L_{OD} is on but L_{OS} is off, hence L_{OD} pulls V_{out} up close to V_{DS} ; ii) when the transistor is working in zone II, with the output-channel connection located within the saturation region on the drain edge; iii) when the transistor is working in zone I so that the channel is turned on, working as a resistor, and the output-channel connection is located in a position to hold a high enough V_{DS} value.

2.3. Proof of Concept Demonstration

In order to demonstrate the suitability of the SMG-MOS logic gates in the fabrication of complex logic circuits, we have implemented our concept to two different kinds of circuits. The first implementation example is a ring oscillator (RO) circuit. The

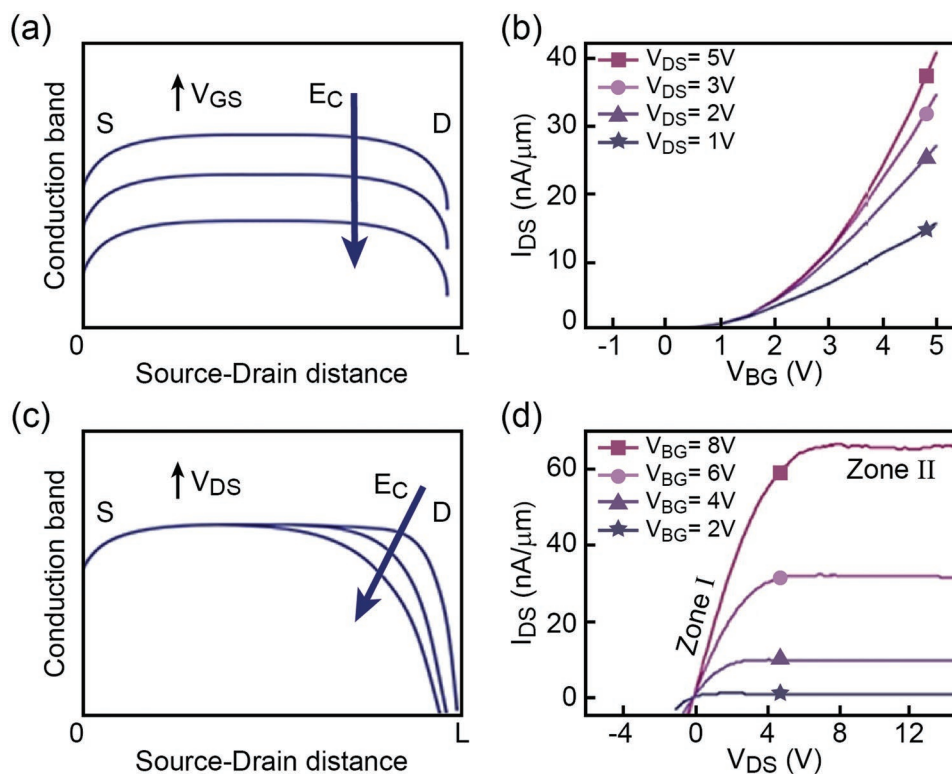


Figure 4. Conduction band explanation of general SMG-MOS logic gates. a) Schematic diagram showing that E_c along the entire channel decreases as the gate voltage V_{GS} increases. b) I_{DS} versus V_{GS} (here V_{BG}) plot suggesting the V_{GS} impact on the channel at varying V_{DS} . c) Schematic diagram showing that only the part of E_c near the drain is bended down when V_{DS} is increased. d) I_{DS} versus V_{DS} plot at varying of V_{GS} (here V_{BG}). In (a,c) the L is the distance between source and drain.

RO plays an important role in microprocessors since it provides the clock signals as a timer to define when each functional unit starts and stops working. A typical RO can be formed by combining different logic NOTs. Here, a five-stage SMG-MOS logic NOT is fabricated with one stage connecting the following stage hence forming the RO circuit as schematically shown in **Figure 5a** (see Experimental Section). The labels V_{DS} , V_{out} , and GND correspond to the supplied voltage, the output voltage, and the source ground voltage, respectively. Figure 5b demonstrates the functionality of the RO. When $V_{DS} = 2$ V, the output voltage oscillates as a function of time. Figure 5c illustrates a SEM image of such device (top view), which was fabricated via a standard lithography procedure suggesting that it could be easily adaptable to foundry lines for mass production. Importantly, already at the lab scale, we could reduce the number of necessary transistors of half with respect to the standard CMOS approach. At present, the SMG-MOS RO showed an oscillation frequency limited only by the intrinsic property of IGZO and the parasitic resistance due to the device dimension.^[55–57] The mobility of the IGZO transistors here is around $1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, which is much lower than poly-Si ($\approx 100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$).^[46] We believe that the oscillation frequency would be enhanced with a proper choice of channel materials and by improving the structure dimensions through more advanced foundry lithography. Even though the illustrated result sounds very promising, it must be highlighted the low resulting voltage output. This is ascribed to the use of the side gate as input instead of the bottom gate, the latter one a solution which could probably

improve the performance of the RO due to the stronger effect of the bottom gate on the SMG-MGO output.

The second implementation example consists of a half adder circuit by making use of AND and XOR logic functions. A half adder circuit can realize the addition of two single binary digits as input 1 and input 2 by producing two outputs, the sum (S or output 1) and the carry (C or output 2). A half adder is important for electronics because two half adders compose a full adder which is a fundamental component in the arithmetic logic. A half adder structure can be realized through the combination of logic AND and XOR gates, i.e., through the employment of two SMG-MOS. A half adder is an adder not taking into consideration the carry from the lower order. A half adder has two inputs and two outputs, the latter formed by the sum value and the carry. When either the input 1 or input 2 is 1, the sum value is 1 with the carry returning 0. When both inputs are 1, the sum is 0 and the carry is 1. The complete truth table for the half adder circuit is shown in **Table 1**.

As shown in **Figure 6a**, a half adder circuit was implemented by employing a SMG-MOS logic AND and a logic XOR. The XOR logic gate standard implementation requires the use of several transistors or, alternatively, of a single SMG-MOS. In **Figure 6a**, the two SMG-MOS logic gates highlighted in blue square blocks share the same drain, source, side gate, and bottom gate. These two SMG-MOS logic gates have the same channel length but two different distances from the side gate to the channel, referred as L_{SC} . In particular, SMG-MOS1 has

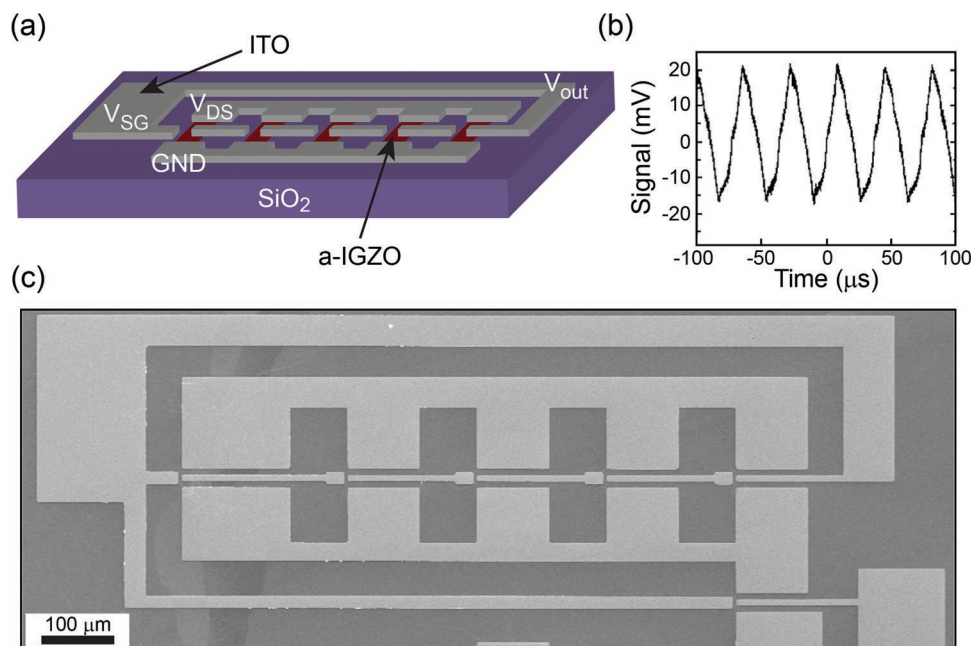


Figure 5. RO circuit. a) Schematic illustration of a five-stage SMG-MOS NOT ring oscillator. b) Output voltage as a function of time for the five-stage SMG-MOS RO at $V_{DS} = 2$ V. c) SEM image of a five-stage SMG-MOS RO (top view).

shorter L_{SC} than SMG-MOS2, resulting in the implementation of XOR logic and AND logic, respectively.

The working mechanism is as follows. As shown in the cross-section of the circuit in Figure 6b, there are generally two different routes for V_{SG} to control the channel: i) control of the bottom of the channel through capacitor C_1 and bottom gate, as shown by the yellow arrow route in the left side of Figure 6b; ii) control of the top or side of the channel through capacitor C_2 , as shown by the blue arrow route in the right side of Figure 6b. In particular, for the logic AND gate, L_{SC} is long enough that the route represented by the blue arrow is not accessible. In this case, V_{SG} controls the channel through the route represented by the yellow arrow, pointing toward the bottom gate voltage. This is consistent with the experimental results depicted in Figure 6c, showing the transfer curve shifting to the left by increasing V_{SG} . For the logic XOR gate shown in Figure 6b, L_{SC} is instead small enough to turn on the blue arrow route. V_{SG} can control the top of the channel, now in the opposite direction of the bottom gate V_{BG} . In this case, when V_{SG} increases, a higher V_{BG} is required to turn on the channel for the same I_{DS} . This is consistent with the experiments in Figure 6d showing a slight shift towards the right (the electric potential values are shown in Figure S6, Supporting Information).

Table 1. Half adder truth table.

Input 1	Input 2	Sum value	Carry
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

Based on this information, the logic XOR can be implemented by adopting the following procedure. To start $V_{SG} = \text{logic } 0$, therefore L_{OD} is inactive when V_{BG} corresponds to logic 0. When instead V_{BG} shifts from logic 0 to logic 1, the channel is activated and $V_{out} = I_{DS} \cdot R_{OS}$ shifts from logic 0 to logic 1 (where R_{OS} is the channel resistance from the output to source). The next situation considers instead $V_{SG} = \text{logic } 1$, situation where L_{OD} is turned on at $V_{BG} = \text{logic } 0$ which results in $V_{out} = \text{logic } 1$. Finally, when also $V_{BG} = \text{logic } 1$ then a relatively smaller I_{DS} is generated leading to $V_{out} = I_{DS} \cdot R_{OS} < \text{logic } 1$ condition (i.e., logic 0). By this reasoning the XOR table truth is formed.

We have seen how the SMG-MOS solution carries a number of advantages toward standard CMOS technology. As for the footprint and thus the area, by using fewer transistors, SMG-MOS structures are smaller than the corresponding CMOS logic gates in the same technology node. In particular, for the 0.13 μm technology node, the SMG-MOS logic NOT footprint results to be around 40% of the standard CMOS-NOT (with the surface area of $\approx 1.84 \mu\text{m}^2$ with effective reduction in the required number of fabrication steps would be achieved. Finally, an evident advantage would result from the instrumentation point of view as the present processing lines, 14 nm CMOS technology node, could allow the realization of SMG-MOS circuits with footprint equivalent to 10 nm CMOS technology node. This possibility sounds especially appealing considering that updating the standard 14 nm to a 10 nm technology node is estimated to require one billion dollars for processing and 0.3 billion for designing.

The SMG-MOS architecture presents an advantage over CMOS also in terms of low power dissipation, protecting circuits from heating, which degrades performance. In general, the static power dissipation of a single transistor is

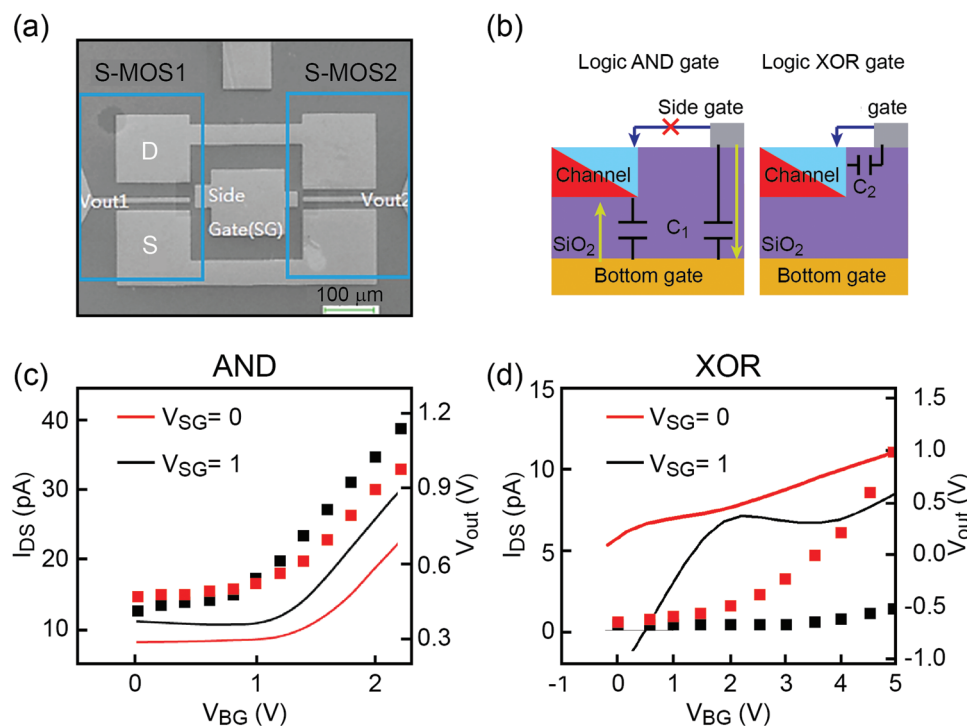


Figure 6. Half-adder circuit. a) SEM image of a half adder with logic XOR (SMG-MOS1) and logic AND (SMG-MOS2). b) Cross-section schematic circuit diagrams of a SMG-MOS looked from the drain side into the channel, with the arrows showing two routes through which V_{SG} controls the channel: i) Yellow arrow: route through capacitors C_1 ; ii) Blue arrow: route through capacitor C_2 . c) Transfer curves for logic AND, showing the transfer current I_{DS} (squares) shifting to the left by increasing V_{SG} . The continuous lines represent V_{out} . The red color stands for $V_{SG} = \text{logic } 0$, black colors for $V_{SG} = \text{logic } 1$. d) Transfer curve for logic XOR. The curve associated to I_{DS} shifts to the right by increasing V_{SG} . Here $V_{BG} = V_{in1}$ and $V_{SG} = V_{in2}$.

proportional to $I_{DS} \cdot V_{DD}$, where V_{DD} is the working voltage. SMG-MOS transistors work in the subthreshold region around 0.7 V (Figure 2c,f–i), so that I_{DS} can be kept lower than the leakage current limit ($100 \text{ nA } \mu\text{m}^{-1}$) and V_{DD} lower than the working voltage limit ($\approx 1.5 \text{ V}$). The limits of $100 \text{ nA } \mu\text{m}^{-1}$ and 1.5 V are required by the International Technology Roadmap for Semiconductors (ITRS), followed by the foundries across the world^[5] (see section Electrical Properties Measurement for further details). Finally, as for the mass production, SMG-MOS is processed via standard lithography and thus relatively easy to adapt into foundry lines with high repeatability and reliability.

3. Conclusions

The advancement of semiconductor technology toward faster and more efficient data processing will soon require innovative technological solutions as the physical limitations of materials is getting closer. In this respect, the conventional scaling down methods show several limitations. For example, CMOS logic gate circuits employing high number of transistors are hard to scale down, while bench-top innovations for advanced miniaturized components cannot always be implemented into common previous product lines quickly or efficiently. Therefore, there is a need for designs, which can be fabricated by employing existing foundry CMOS technologies. The SMG-MOS design presented herein has demonstrated the efficiency and flexibility

of executing multiple logic gate functions. SMG-MOS logic gates carry the important advantage in reducing footprint and costs (in time, materials, and processing steps) required to achieve the same function of CMOS logic gates. In addition, the SMG-MOS logic gates have a lower static power consumption with respect to CMOS logic gates. As demonstration, we have implemented a ring oscillator circuit by using SMG-MOS logic NOTs, with the result of reducing the transistor number by half when compared to a standard ring oscillator circuit realized with CMOS logic NOTs. As a further example, SMG-MOS can also be used as data calculator circuits for data processing in IC such as half adders. Finally, no particular requirement needs to be added to conventional semiconductor processing for SMG-MOS, which suggests that SMG-MOS can be adopted by the existing semiconductor foundry lines. Owing to the simplicity of the design, its low power consumption and low cost, the SMG-MOS concept could represent a new possible way to scale down electronics circuits.

4. Experimental Section

Materials: A layer of SiO_2 with thickness $100 \pm 20 \text{ nm}$ acting as insulator layer was grown on the surface of n-type silicon. The employed Si wafer was characterized by a 2 in. diameter, crystal orientation $\langle 100 \rangle$, resistance less than $0.005 \text{ } \Omega \text{ cm}^2$ with thickness of $400\text{--}500 \text{ } \mu\text{m}$. Substrates were purchased from Suzhou Yancai Micro-nano Sciencetech Corp. (Taipei, Taiwan, China). Indium–gallium–zinc oxide (IGZO) and Ni/Au (Beijing Founder Star Science and Technology Co., Ltd., China) were deposited and patterned in sequence on the SiO_2/Si wafer. Ni/Au

was used as electrodes due to the good adhesive property of Ni and good electric conductivity of Au.

Fabrication: A 30 nm thick IGZO film was sputtered using a Manual Radio Frequency Magnetron Sputterer at 100 W from Sky Technology Development (Shenyang, China) with a 0.9 Pa working pressure (Ar:O₂ = 14 sccm:3 sccm) at 50 °C. The resulting channel width and length were ≈15–100 and 30–120 μm, respectively (see Figure 2e). The channel was submitted to a 20 h 200 °C annealing process. Afterwards, Ni/Au metal electrodes of ≈12–60 nm thickness were deposited by MUE-ECO electron-beam-evaporation using an E-beam evaporator from ULVAC (Redwood City, CA, USA). The pressure was 1.8×10^{-3} Pa, and deposition rate no less than 0.06 nm s⁻¹. Finally, the electrodes for the output (O), source (S), drain (D), and side gates (SG) were patterned by lithography with a resolution of 1 μm. In terms of best resolution, by employing a Focus Ion Beam the smallest achievable length between the drain and output was 1 μm with 200 nm width.

Electrical Measurements: The I–V characteristics were measured using a semiconductor parameter analyzer (Keithley 4200), where the source voltage was set to ground (i.e., 0 V). For I_{DS}–V_{GS} measurements, i.e., the typical transfer curves, the drain voltage V_{DS} was set in the range 1.0–1.5 V. The low leakage, hence the low static power dissipation, is explained in more details as follows: i) I_{DS} at input = 0 and 1 is much lower than 100 nA μm⁻¹, as shown in Figure 2c. 100 nA μm⁻¹ is the leakage current limit required by the IC International Technology Roadmap for Semiconductors (ITRS) after scaling down for the present technology node.^[5] ii) The drain voltage used in the SMG-MOS is in the range of 1–2 V, which is the typical working voltage according to ITRS.^[5] iii) The static power dissipation for a single device is the product of channel current and drain voltage (I_{DS}·V_{DD}). Therefore, given the three aforementioned considerations, the static power consumption of a SMG-MOS logic NOT will be comparable to or even lower than the power consumption required by a traditional CMOS NOT.

The Ni/Au metal electrode-IGZO channel contact was also investigated.^[58–60] As shown in Figure S7 (Supporting Information), both the role of the IGZO thickness and the resistance of the metal-IGZO contact were investigated. The experiments suggest an ohmic contact between metal and IGZO, as highlighted by the linear relationship between current and voltage. More details can be found in the Supporting Information.

Another important aspect that was taken into consideration is the effect of the side gate on the transfer curve of the SMG-MOS as might result in an important parameter for controlling the transistor electrical properties. Indeed, as shown in Figure S8 (Supporting Information), the side gate was found to be capable of significantly increase the drain current.

Furthermore, because the static power dissipation is proportional to the number of transistors *n* in the logic gate, the power dissipation in other SMG-MOS logic gate designs could be smaller than that of CMOS logic gate for the same technology nodes, because of fewer transistors. The logic NOT function is repeatable in our samples for more than 10 devices. The OR, AND, NAND, NOR functions are also repeatable. The RO functions are measured in more than five samples in one wafer.

Finally, stability measurements to address the sensitivity of IGZO from the surrounding ambient were performed. In particular, as shown in Figure S9 (Supporting Information), a solution was introduced to minimize the effect of the ambient temperature.

Simulations: The single-transistor circuit structure was simulated by TCAD as follows: First, the mesh was defined by splitting the channel into 50 equally sized slices of 1 μm each (total length 50 μm), and the spatial structure of device was formed. A conductive layer as bottom gate was used as a substrate, onto which silicon oxide was considered. A 40 nm thick n-type channel was then added on top, with doping concentration of ≈10¹⁸ cm⁻³. The side gates, source, and drain contacts were then realized. Subsequently, the physical properties for semiconductor and dielectrics materials could be specified, including mobility (≈1–10 cm² V s⁻¹), subgap density states of holes and electrons (10¹⁸–10²¹ cm⁻³ eV⁻¹), energy bandgap at room temperature (≈3.0 eV) and the Shockley–Read–Hall recombination time for holes and electrons (≈10⁻⁸ s). Afterward, models based on semiconductor device theories

were defined.^[3,4] by including the recombination model, tunneling model, the output-to-drain electric field linkage condition introduced by the special design, and the device degradation model based on hot carrier injection. Defects were also defined by employing the density of states model^[50–52] while the employed material parameters (Figure S5, Supporting Information) were taken from published data.^[50,52,53] Finally, the bias conditions including the voltage applied at drain, source and gate were defined, and the full Newton method was employed to numerically calculate the electrical properties of the illustrated devices.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This work was supported by the National Natural Science Foundation of China (Grant No. 61574147), Zhejiang Provincial Natural Science Foundation for Distinguished Young Scholar (Grant No. LR17F040002), Instrument Developing Project of the Chinese Academy of Sciences (Grant No. YJKYYQ20180021). J.C. acknowledges CAS-TWAS President's Fellowship funding.

Conflict of Interest

The authors declare no conflict of interest.

Keywords

amorphous oxide semiconductors (AOSs), In–Ga–Zn–O (IGZO), integrated circuits, logic gates, metal-oxide-semiconductor field-effect transistors (MOSFETs)

Received: May 21, 2019
Revised: October 17, 2019
Published online: January 24, 2020

- [1] T. P. Ma, *IEEE Trans. Electron Devices* **1998**, *45*, 680.
- [2] Y. K. Choi, K. Asano, N. Lindert, V. Subramanian, T. J. King, J. Bokor, C. Hu, *IEEE Electron Device Lett.* **1999**, *21*, 919.
- [3] Y. S. Chauhan, D. Lu, S. Venugopalan, S. Khandelwal, J. P. Duarte, N. Paydavosi, N. Ai, C. Hu, *FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG Standard*, Academic Press, London, UK **2015**.
- [4] Y. Taur, T. H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, Cambridge, UK **2013**.
- [5] 2013 Update Overview at International Technology Roadmap for Semiconductors, <http://www.itrs2.net/>, (accessed: October 2019).
- [6] S. L. Han, K. Choi, S. K. Jin, S. Yu, K. R. Ko, S. Im, *ACS Appl. Mater. Interfaces* **2017**, *9*, 15592.
- [7] S. Banerjee, S. Garg, S. Saurabh, *IEEE Electron Device Lett.* **2018**, *39*, 773.
- [8] Z. Wang, Y. Zhong, C. Chen, L. Ye, Q. Huang, L. Yang, Y. Wang, R. Huang, presented at *IEEE Int. Symp. Circuits Syst.*, Sapporo, Japan, May **2019**.
- [9] M. M. Shulaker, G. Hills, N. Patil, H. Wei, H. Y. Chen, H. S. Wong, S. Mitra, *Nature* **2013**, *501*, 526.
- [10] J. S. Heo, T. Kim, S. G. Ban, D. Kim, J. H. Lee, J. S. Jur, M.-G. Kim, Y.-H. Kim, Y. Hong, S. K. Park, *Adv. Mater.* **2017**, *29*, 1701822.

- [11] A. G. Shulga, V. Derenskiy, J. M. Salazar-Rios, D. N. Dirin, M. Fritsch, M. V. Kovalenko, U. Scherf, M. A. Loi, *Adv. Mater.* **2017**, 29, 1701764.
- [12] J. Tang, Q. Cao, G. Tulevski, K. A. Jenkins, L. Nela, D. B. Farmer, S.-J. Han, *Nat. Electron.* **2018**, 1, 191.
- [13] J. Zou, K. Zhang, W. Cai, T. Chen, A. Nathan, Q. Zhang, *Nanoscale* **2018**, 10, 13122.
- [14] W. J. Yu, Z. Li, H. Zhou, Y. Chen, Y. Wang, Y. Huang, X. Duan, *Nat. Mater.* **2013**, 12, 246.
- [15] M. Chhowalla, D. Jena, H. Zhang, *Nat. Rev. Mater.* **2016**, 1, 16052.
- [16] F. Horst, A. Farokhnejad, Q.-T. Zhao, B. Iniguez, A. Kloe, *IEEE Trans. Electron Devices* **2019**, 66, 132.
- [17] G. Gao, B. Wan, X. Liu, Q. Sun, X. Yang, L. Wang, C. Pan, Z. Lin Wang, *Adv. Mater.* **2018**, 30, 1705088.
- [18] G. V. Resta, Y. Balaji, D. Lin, I. P. Radu, F. Catthoor, P. E. Gaillardon, G. De Micheli, *ACS Nano* **2018**, 12, 7039.
- [19] N. Ofek, A. Petrenko, R. Heeres, P. Reinhold, Z. Leghtas, B. Vlastakis, Y. Liu, L. Frunzio, S. M. Girvin, L. Jiang, *Nature* **2016**, 536, 441.
- [20] T. R. Tan, J. P. Gaebler, Y. Lin, Y. Wan, R. Bowler, D. Leibfried, D. J. Wineland, *Nature* **2015**, 528, 380.
- [21] M. Veldhorst, C. H. Yang, J. C. Hwang, W. Huang, J. P. Dehollain, J. T. Muhonen, S. Simmons, A. Laucht, F. E. Hudson, K. M. A. Itoh, *Nature* **2015**, 526, 410.
- [22] C. J. Ballance, T. P. Harty, N. M. Linke, M. A. Sepiol, D. M. Lucas, *Phys. Rev. Lett.* **2016**, 117, 060504.
- [23] S. Weidt, J. Randall, S. C. Webster, K. Lake, A. E. Webb, I. Cohen, T. Navickas, B. Lekitsch, A. Retzker, W. K. Hensinger, *Phys. Rev. Lett.* **2016**, 117, 220501.
- [24] K.-K. Ni, T. Rosenband, D. D. Grimes, *Chem. Sci.* **2018**, 9, 6830.
- [25] V. M. Schäfer, C. J. Ballance, K. Thirumalai, L. J. Stephenson, T. G. Ballance, A. M. Steane, D. M. Lucas, *Nature* **2018**, 555, 75.
- [26] A. J. Genot, A. Baccouche, R. Sieskind, N. Aubertkato, N. Bredeche, J. F. Bartolo, V. Taly, T. Fujii, Y. Rondelez, *Nat. Chem.* **2016**, 8, 760.
- [27] P. Siuti, J. Yazbek, T. K. Lu, *Nat. Biotechnol.* **2013**, 31, 448.
- [28] T. S. Moon, C. Lou, A. Tamsir, B. C. Stanton, C. A. Voigt, *Nature* **2012**, 491, 249.
- [29] J. Bonnet, P. Yin, M. E. Ortiz, P. Subsoontorn, D. Endy, *Science* **2013**, 340, 599.
- [30] B. Wang, R. I. Kitney, N. Joly, M. Buck, *Nat. Commun.* **2011**, 2, 508.
- [31] A. M. Ionescu, H. Riel, *Nature* **2011**, 479, 329.
- [32] T. Huff, H. Labidi, M. Rashidi, L. Livadaru, T. Dienel, R. Achal, W. Vine, J. Pitters, R. A. Wolkow, *Nat. Electron.* **2018**, 1, 636.
- [33] B. A. Badeau, M. P. Comerford, C. K. Arakawa, J. A. Shadish, C. A. DeForest, *Nat. Chem.* **2018**, 10, 251.
- [34] S. Joo, T. Kim, S. H. Shin, J. Y. Lim, J. Hong, J. D. Song, J. Chang, H.-W. Lee, K. Rhie, S. H. Han, K.-H. Shin, M. Johnson, *Nature* **2013**, 494, 72.
- [35] D. Skidin, O. Faizy, J. Krüger, F. Eisenhut, A. Jancarik, K.-H. Nguyen, G. Cuniberti, A. Gourdon, F. Moresco, C. Joachim, *ACS Nano* **2018**, 12, 1139.
- [36] S. Wang, C. Chen, Z. Yu, Y. He, X. Chen, Q. Wan, Y. Shi, D. W. Zhang, H. Zhou, X. Wang, P. Zhou, *Adv. Mater.* **2019**, 31, 1806227.
- [37] Z. Q. Wang, H. Y. Xu, X. H. Li, H. Yu, Y. C. Liu, X. J. Zhu, *Adv. Funct. Mater.* **2012**, 22, 2759.
- [38] C. X. Wu, T. W. Kim, H. Y. Choi, D. B. Strukov, J. J. Yang, *Nat. Commun.* **2017**, 8, 752.
- [39] Q. Z. Liu, Y. H. Liu, J. Li, C. Lau, F. Q. Wu, A. Y. Zhang, Z. Li, M. R. Chen, H. Y. Fu, J. Draper, X. Cao, C. W. Zhou, *ACS Appl. Mater. Interfaces* **2019**, 11, 16749.
- [40] J. M. Zhou, N. Liu, L. Q. Zhu, Y. Shi, Q. Wan, *IEEE Electron Device Lett.* **2015**, 36, 198.
- [41] Y. N. Zhong, T. Wang, X. Gao, J. L. Xu, S. D. Wang, *Adv. Funct. Mater.* **2018**, 28, 1800854.
- [42] Y. H. Liu, L. Q. Zhu, P. Feng, Y. Shi, Q. Wan, *Adv. Mater.* **2015**, 27, 5599.
- [43] J. T. Yang, C. Ge, J. Y. Du, H. Y. Huang, M. He, C. Wang, H. B. Lu, G. Z. Yang, K. J. Jin, *Adv. Mater.* **2018**, 30, 1801548.
- [44] C. J. Wan, Y. H. Liu, P. Feng, W. Wang, L. Q. Zhu, Z. P. Liu, Y. Shi, Q. Wan, *Adv. Mater.* **2016**, 28, 5878.
- [45] C. J. Wan, B. J. Li, P. Feng, L. Q. Zhu, Y. Shi, Q. Wan, *IEEE Trans. Electron Devices* **2016**, 63, 3958.
- [46] E. Fortunato, P. Barquinha, R. Martins, *Adv. Mater.* **2012**, 24, 2945.
- [47] M. D. H. Chowdhury, P. Migliorato, J. Jang, *Appl. Phys. Lett.* **2013**, 103, 152103.
- [48] M. Estrada, M. Rivas, I. Garduño, F. Avila-Herrera, A. Cerdeira, M. Pavanello, I. Mejia, M. A. Quevedo-Lopez, *Microelectron. Reliab.* **2016**, 56, 29.
- [49] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, H. Hosono, *Nature* **2004**, 432, 488.
- [50] M. Kimura, T. Nakanishi, K. Nomura, T. Kamiya, H. Hosono, *Appl. Phys. Lett.* **2008**, 92, 133512.
- [51] H. H. Hsieh, C. H. Wu, C. C. Wu, Y. H. Yeh, H. L. Tyan, C. M. Leu, *SID Symp. Dig. Tech. Pap.* **2008**, 39, 1207.
- [52] M. Dai, N. Dai, *Nano Lett.* **2012**, 12, 5954.
- [53] M. Dai, W. Xu, *Appl. Phys. Lett.* **2012**, 100, 501.
- [54] Q. Xie, C. J. Lee, J. Xu, C. Wann, Y. C. Sun, T. Yuan, *IEEE Trans. Electron Devices* **2013**, 60, 1814.
- [55] K. H. Cherenack, B. Hekmatshoar, J. C. Sturm, S. Wagner, *IEEE Trans. Electron Devices* **2010**, 57, 2381.
- [56] W. Fix, A. Ullmann, J. Ficker, W. Clemens, *Appl. Phys. Lett.* **2002**, 81, 1735.
- [57] Y. H. Kim, J. S. Heo, T. H. Kim, S. Park, M. H. Yoon, J. Kim, M. S. Oh, G. R. Yi, Y. Y. Noh, S. K. Park, *Nature* **2012**, 489, 128.
- [58] M. J. Choi, M. H. Kim, D. K. Choi, *Appl. Phys. Lett.* **2015**, 107, 053501.
- [59] N. K. Cho, J. Park, D. Lee, J. W. Park, W. H. Lee, Y. S. Kim, *ACS Appl. Electron. Mater.* **2019**, 1, 1698.
- [60] E. Lee, J. Lee, J. H. Kim, K. H. Lim, J. S. Byun, J. Ko, Y. D. Kim, Y. Park, Y. S. Kim, *Nat. Commun.* **2015**, 6, 6785.